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| **EDUCATIONAL QUALIFICATION** | | | |
| **Year** | **Degree** | **Institution/ School** | **Performance** |
| 2018 | B.E (Electronics and Communication Eng.) | J.S.S Academy of Technical Education Bangalore | 67.5% |
| 2015 | Diploma(Electronics and Communication Eng.) | B.V.V.S Polytechnic Bagalkot | 77.44% |
| 2012 | Class X | S.S.S.B.V.V.S Hi-School Halingali | 82.72% |

**PROFESSIONAL TRAINING**

* **Advance VLSI Design and Verification training.** [ Jan’18 – Jun’18 ]

Maven Silicon Bangalore.

**PROFESSIONAL SKILLS**

UVM | SV | SVA | OOPS Concept | Verilog | STA | Digital Electronics | Perl | C.

**TOOLS**

Linux | GVIM | Cadence SimVision | Vmanger | Design Sync |Questasim | Modelsim | Quartus Prime | EDA Playground

**PROFESSIONAL EXPERIENCE**

**Senior Design Verification Engineer, ExcelMax Bangalore [Jun’**2018 – 2023**]**

**Profession Summary:**

* Experience in developing Verification plan, Implementation test plan documents
* Experience in developing System Verilog, UVM-based Verification environments and testbench components including agents, drivers and scoreboard.
* Experience in writing Tests and Sequences with Constrained-Random stimulus.
* Good Knowledge on UART and I2C Protocol.
* Good Knowledge on Assertion.
* Worked Code coverage.
* Debugging .

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| **PROJECTS** |

## Verification of TDM switch for Modem:

* TDM switch is used to make use of the bandwidth of channels with maximum efficiency via shared interface pipes. It Supports E1 bit rate and time slots (32 time slots or 32 DSO channels at bit rate 2.048Mbps).
* Created Verification plan.
* Developed SV-UVM based verification plug & play env.
* Created testcase sequences to verify various key features.
* Analyzed toggle coverage.
* Worked on code model.
* Closed Code coverage as 100%

## UART IP Veriﬁcation:

* The UART IP core provides serial communication capabilities, which allows communication with modem or other external devices.
* Implemented an Baudrate generation block.

## Veriﬁcation:

* Verified the design using UVM TB Architecture blocks i.e. Agents, Environment and Tests in QuestaSim.
* Verified the UART packet of 5,6,7,8bits. Prity and Different baudrate also verified using UVM TB.
* Verified the RTL module using Verilog TB.

## Router 1x3 Design and Veriﬁcation:

* The router accepts data packets on a single 8-bit port and routes them to one of the three output channels - channel0, channel1, and channel2.It's a 3-layered network device as per the OSI reference model of the network.
* Implemented various submodules i.e. FSM, FIFO, Register and Synchronizer using Verilog HDL.
* Implemented the Synthesizable design circuit using Quartus Prime.

## Veriﬁcation:

* Verified the design using UVM TB Architecture blocks i.e. Agents, Environment and Tests in QuestaSim.
* Connected the design and verification environment using interface and virtual interface.

## RAM Verification Project:

* Designed and Verified 16x8 synchronous dual port RAM memory and single RAM Memory. The Memory model is capable of storing and retrieving 16bits of data as per address location.
* Perform write to any memory location, read from the same memory location, read data should be the same as written data
* Assert reset in between write/read operation and check for default values.
* Verified the design using functional coverage by defining covergroups and coverpoints.

## APB VIP Verification Using UVM:

* APB is designed for low bandwidth control accesses, for example peripheral interfaces on system. This bus has an address and data phase but a much reduced, low complexity signal list. Furthermore, it is an interface designed for a low frequency system with a low bit width (32 bits)
* AMBA-APB protocol specification.
* Created Verification Plan.
* Created Verification Environment using UVM Methodology
* Worked on Write & Read Sequence, Driver, Monitor, Scoreboard
* Performed read and write operations with and without wait states. Also, Slave Error Situation.

## FIFO Verification :

* Develop a comprehensive testbench environment to verify the functionality and performance of the FIFO design.
* Perform functional simulation, checking for proper data flow, synchronization, and handling of empty and full conditions.
* Debug and resolve design or verification-related problems, ensuring the FIFO operates correctly according to the specifications.
* Created Verification Plan.
* Created Verification Environment using SV Test Bench.
* Worked on Testcase writing, Generator, Driver, Monitor.

# HOBBIES

Cricket **I** Kabaddi **I** Cooking

**LANGUAGES**

Kannada **I** English **I** Hindi **I** Telugu.

**DECLARATION**

I, hereby declare that the information furnished above is correct to the best of my knowledge.

Date:

Place: Bangalore [Bharamu S K]